## ABSTRACT OF THE DISCLOSURE

# METHOD AND SYSTEM FOR ANALYZING QUIESCENT POWER PLANE CURRENT (IDDQ) TEST DATA IN VERY-LARGE SCALE INTEGRATED (VLSI) CIRCUITS

A method and system for analyzing quiescent power plane current test data in a very large scale integrated (VLSI) circuit provides diagnostic information and improved IDDQ testing for analyzing and detecting manufacturing defects in a VLSI device. A set of IDDQ test values is collected over a set of test vectors for a group of devices. Values that are detected as corresponding to activated defects (e.g., shorts) are discarded from the data set and the data set is checked for correlation between the remaining ostensibly defect-free data values and devices (or alternatively vectors) that do not correlate are discarded from the data set. Then, a regression is generated for each vector from and IDDQ values for each vector and the IDDQ values at a selected reference vector (excepting the reference vector). Next, the IDDQ values at each vector for each device are normalized by estimating an expected IDDQ value for that vector and device from the regression for the vector and the device's measured reference vector IDDQ value. A cross-correlation check is performed to determine whether the set of measurements represents a good set of ostensibly defect-free measurements. New values that are detected as corresponding to an activated defect are discarded and previously discarded values are potentially reclaimed. The above regression, normalization and discard procedure is repeated until the set of non-defect activated vectors is stable and the IDDQ measurements can be categorized into discrete categories. The categorized

IDDQ values may be used for identifying and potentially diagnosing defective devices and/or acceptability of devices can be determined from the normalized IDDQ values.